FORM PTO-1390 (REV. 11-2000) U.S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY 'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		015057-091620US
		U.S. APPLICATION NO. (If known, see 37 CFR 1 5) 09/857453
INTERNATIONAL APPLICATION NO. PCT/US99/28230	INTERNATIONAL FILING DATE November 29, 1999	PRIORITY DATE CLAIMED December 4, 1998

TITLE OF INVENTION
MULTIPLE-THICKNESS GATE OXIDE FORMED BY OXYGEN IMPLANTATION

APPLICANT(S) FOR DO/EO/US
YA-CHIN KING; TSU-JAE KING; CHEN MING HU

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST submission of items concerning a filing under 35 U.S.C. 371.**
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 36 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f). The submission must include items (5), (6), (9) and (21) indicated below.
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 37(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau
   c. ☒ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.2 and 35 U.S.C. 1.821 – 1.825.
18. ☐ A second copy of the published international application under 36 U.S.C.
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information:

I/S/ Application no. (if known, see 37 CFR 1.5) 09/857453	INTERNATIONAL APPLICATION NO PCT/US99/28230	ATTORNEY'S DOCKET NUMBER 015057-091620US

21. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492(A) (1) – (5)):	CALCULATIONS PTO USE ONLY	
Neither international preliminary examination fee (37 CFR 1.492) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search report prepared by the EPO of JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$690**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	$	
Total claims	20 - 20 =		x **$18.00**	$	
Independent claims	5 -3 =	2	x **$80.00**	**$160**	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **270.00**	$	
			TOTAL OF ABOVE CALCULATIONS =	**$850**	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$	
			SUBTOTAL =	**$850**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFT 1.492(f).				$	
			TOTAL NATIONAL FEE =	**$850**	
Fee for recording the enclosed assignment (37 CFR 1.2(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$	
			TOTAL FEES ENCLOSED =	**$850**	
			Amount to be refunded:	$	
			charged:	$	

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 20-1430 in the amount of $850 to cover the above fees.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-1430. A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Henry K. Woodward
Townsend and Townsend and Crew LLP
Two Embarcadero Center, 8th fl.
San Francisco, CA 94111

SIGNATURE

J. Georg Seka
NAME

24,491
REGISTRATION NUMBER

MULTIPLE-THICKNESS GATE OXIDE FORMED BY OXYGEN IMPLANTATION

BACKGROUND OF THE INVENTION

The present invention relates to the manufacture of electronic devices, particularly semiconductor devices, such as logic circuits, memory circuits, and/or combinations thereof.

Electronic devices are being made that combine various types of circuits on a single chip of semiconductor material. For example, devices are being made that combine logic circuits with memory arrays, or various types of memory, so that higher functionality can be achieved on a single chip. This type of integration often provides lower cost, smaller size and improved reliability compared to achieving the same functionality with a number of different chips wired together. Unfortunately, it can be difficult to integrate the manufacture of one type of circuit with another on a single chip.

Different types of circuits might have different types of devices that require different voltage inputs, and that have different thickness of gate oxide. For example, a logic field-effect transistor ("FET") might have a different gate oxide thickness than an electronically erasable-programmable read only memory cell, or than a dynamic read-addressable memory ("DRAM") cell. It is generally desirable to make all the gate oxides for all the devices on the chip in a single process step; therefore, it may be necessary to make the gate oxide in some regions thinner than the gate oxide in other regions.

A technique has been used to vary the thickness of an oxide layer grown on a silicon wafer during a oxide growth process by implanting nitrogen into selected regions of the silicon. The implanted nitrogen retards the growth of silicon oxide, resulting in a gate oxide of diminished thickness where the nitrogen was implanted. However, implanting nitrogen can degrade the resultant quality of the gate oxide. Gate oxide quality is especially important, compared to an inter-metal dielectric layer, for

example, because of the electric field gradients a gate oxide must withstand and the low current leakage that is generally desired for good device performance. The quality of the gate oxide becomes even more important as device geometry and operating voltages shrink, both of which are associated with thinner gate oxides.

Therefore, it is desirable to fabricate an electronic device die with multiple thicknesses of gate oxide, and it is further desirable to be able to fabricate gate oxides of superior quality, especially thin gate oxides.

SUMMARY OF THE INVENTION

According to the present invention a multiple-thickness oxide layer may be grown by implanting oxygen into selected regions of a substrate where a thicker oxide layer is desired. In one embodiment, oxygen is implanted into selected regions of a silicon substrate through a thin sacrificial layer at an energy between about 10-30 keV. The sacrificial layer reduces implantation damage to the underlying silicon, and is stripped prior to thermal oxidation of the substrate, and the resulting oxide layer has multiple thickness and is of high quality and is suitable for a gate dielectric, for example.

In another embodiment, a polysilicon layer between about 1,000-5,000 Å thick is deposited over a gate oxide prior to implanting oxygen into selected regions of the silicon substrate. The implant energy is chosen according to the thickness of the polysilicon layer to place the peak of the oxygen profile just above the gate oxide. The substrate is then annealed in a nitrogen ambient at a temperature of about 900 °C for about 30 minutes to grow a thicker oxide in the regions that were implanted with oxygen.

Implanting oxygen to increase oxide thickness can provide a differential thickness of about 5-20 Å for implant doses of between about 5E15/cm^2-1E16/cm^2. Unlike nitrogen implantation techniques, where the thickness differential is highly sensitive to the thickness of the oxide, the present invention provides a differential thickness that is less sensitive to the oxide thickness. Additionally, the oxygen-implanted oxides exhibit superior reliability to nitrogen-implanted oxides, and even non-implanted oxides.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A-1C are simplified cross sections of a semiconductor die illustrating a fabrication sequence resulting in multiple oxide thicknesses using an oxygen

implant performed prior to gate oxidation, according to an embodiment of the present invention;

Figs. 1D-1F are simplified cross sections of a semiconductor die illustrating a fabrication sequence resulting in multiple oxide thicknesses using an oxygen implant performed after a polysilicon deposition, according to another embodiment of the present invention;

Fig. 2 is a graph illustrating the oxide thickness differential between implanted and unimplanted regions for oxygen implants and nitrogen implants versus unimplanted oxide thickness;

Fig. 3 is a graph illustrating the tunneling current characteristics of gate oxides formed in accordance with the fabrication sequence illustrated in Figs. 1A-1C and an unimplanted gate oxide;

Fig. 4 is a graph showing the capacitance versus gate voltage for the samples shown in Fig. 3;

Fig. 5 is a graph illustrating the tunneling current characteristics of gate oxides formed in accordance with the fabrication sequence illustrated in Figs. 1D-1F and an unimplanted gate oxide;

Fig. 6 is a graph showing the capacitance versus gate voltage for the samples shown in Fig. 5;

Fig. 7 is a graph of drain current versus gate voltage for various oxide layers at various drain bias voltages;

Fig. 8 is a graph of charge-to-breakdown versus stress current for relatively thin oxide layers fabricated with nitrogen implant technology and for oxide layers fabricated with oxygen implant technology of comparable thicknesses;

Fig. 9 is a graph of charge-to-breakdown versus stress current for relatively thick oxide layers fabricated with nitrogen implant technology and for oxide layers fabricated with oxygen implant technology of comparable thicknesses;

Fig. 10 is a bar chart of charge-to-breakdown at a constant stress current density for oxides of various thicknesses made using a nitrogen implantation method, oxygen implantation methods, and no implantation;

Fig. 11 is a graph of drain current degradation versus injected charge for oxide layers of comparable thickness using a nitrogen implantation technique, an oxygen implantation technique, and no implant.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

As noted above, the present invention provides an improved multiple-thickness gate oxide for transistors on a single semiconductor die.

Figs. 1A-1C and Figs. 1D-1E illustrate steps for two embodiments of the invention in forming multiple gate oxide thicknesses. In Fig. 1A a silicon substrate 10 has a layer of LOCOS silicon oxide 12 on a surface with a layer of photoresist formed over a portion of oxide 12 to limit implantation of oxygen at 16. Thereafter, in Fig. 1B the photoresist and thin LOCOS oxide are striped, and in Fig. 1C gate oxide, T_{OX1} and T_{OX2}, are grown on the surface. T_{OX2} over the heavier implanted oxygen is thicker than T_{OX1} over the lighter implanted (or non-implanted) oxygen. Gate oxidation is carried out at 800°C followed by a two hour anneal at 500°C. Source and drain anneal is carried out later at 900°C for 30 minutes.

The steps in the second embodiment illustrated in Figs. 1D-1F are similar to the steps in the first embodiment, but the oxygen implant 16 is after the polysilicon gate 18 deposition to prevent damage and contamination of the substrate. Again, photoresist 14 is utilized to vary or prevent the oxygen implant.

Previous studies of forming thicker gate oxides using large implant dose of oxygen ($\sim 10^{17} - 2\times10^{18}$ cm^{-2}) have shown that severe damage occurs in the substrate, casting oxygen implant as an unsuitable technique for forming gate oxides. Due to the scaling of the gate oxide, however, the thickness differentials in today's embedded circuits is less than 5 nm as illustrated in the following table:

Circuit	Gate Voltage	Gate Oxide Thickness
Logic	1.5 V	30 Å
I/O	2.5 V	50 Å
DRAM	2.0 V	40 Å
EEPROM	-8 V	80 Å

Fig. 2 is a graph illustrating oxide thickness without implant and the resulting oxide thicknesses with oxygen implant and with nitrogen implant. Fig. 2 shows that the oxide thickness differential created with a nitrogen implant strongly depends on

the unimplanted oxide thickness. In contrast, the thickness differential is independent of the unimplanted T_{ox} when the oxygen implant is used.

Fig. 3 plots gate voltage (V) versus gate current (A/cm^2) and illustrates the tunneling current characteristics for the gate oxide formed with oxygen implant using the process of Figs. 1A-1C. The physical thicknesses were extracted by comparing the measured current with the theoretical tunneling current and were confirmed by pairing the measured high frequency CV data with simulated results from a 1-D self-consistent Shrodinger and Poisson equations solver, as illustrated in Fig. 4. It was found that as the oxygen implant dose increases, the substrate doping level and thus $\|V_t\|$ also rises as a result of thermal donor generation from excess oxygen in the substrate. This effect can be eliminated by optimizing the anneal steps. Figs. 5 and 6 are similar to Figs. 3 and 4 and show that similar increases in oxide thickness are also achieved with oxygen implanted after polysilicon deposition. The good agreement of the measured IV and CV data with theory in Figs. 3-6 demonstrates that neither the interface nor the bulk property of the oxide is compromised by the oxygen implant.

Fig. 7 is a plot of gate voltage (V) versus drain current (A) and illustrates the subthreshold characteristics of transistors with gate oxide formed from various oxygen implant doses. No degradation in subthreshold swing or excessive leakage was observed in devices fabricated with the oxygen implant technology of the present invention.

Figs. 8 and 9 are plots of stress current (A/cm^2) versus change to breakdown ($Coul/cm^2$) and illustrate the reliability of the oxides grown by oxygen implant as compared with those formed by nitrogen implant. Figs. 8 and 9 show that 20 Å/30 Å and 30 Å/50 Å multiple oxide technologies using oxygen implant yield significantly larger Q_{BD} than the nitrogen implant technology. Fig. 10 shows that oxygen implanted oxides have even better Q_{BD} than the conventional oxide while nitrogen implanted oxides have significantly lower Q_{BD}. The Q_{BD} of each thickness group was measured at the same stress currently density. In Fig. 11, oxides with the oxygen implant showed smaller drain current degradation after Fowler-Nordheim current stressing.

In another embodiment of the invention, the process illustrated in Figs. 1D-1E includes the deposition of a high dielectric constant layer at the silicon substrate surface prior to the deposition of the polysilicon gate 18. A suitable high dielectric

constant layer can be a silicon nitride, zirconium oxide, or hafnium silicate (HfSiO). Thereafter, oxygen implantation into the silicon substrate and/or polysilicon gate followed by annealing, as in the process of Figs. 1D-1F, will grow a very thin (<2 nm) silicon oxide with well-controlled thickness. The thin silicon oxide can serve as the buffer layer or interfacial layer that is critical to the attainment of high carrier mobility and low interface defects. In the prior art, the buffer layer is deposited or grown in an oxygen gas atmosphere with buffer layer thickness difficult to control.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. For example, while reference is made to "O_2" implants, it is understood that the implant is done with an O^+ oxygen ion, or other types of oxygen, such as oxygen plasma species, or radicals, or even oxygen containing compounds, such as OH^-, might be used to implement the present invention. Similarly, although the invention has been described in terms of a silicon substrate, it is understood that such a silicon substrate might be a single-crystal silicon wafer, a silicon-on-insulator wafer, a silicon-containing substrate, or the like. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention, which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. A method of forming a multiple-thickness oxide layer on a silicon substrate, the method comprising:

a) forming a sacrificial oxide layer on the silicon substrate;

b) patterning an implant mask layer on the silicon substrate to expose a selected first portion of the silicon substrate;

c) implanting oxygen into the selected first portion of the silicon substrate through the sacrificial oxide layer;

d) stripping the implant mask layer from the silicon substrate;

e) stripping the sacrificial oxide layer; and

f) growing an oxide layer on the silicon substrate, the oxide layer having an oxygen-implanted oxide region and a non-implanted oxide region.

2. The method of claim 1 wherein the non-implanted oxide region is less than about 30 Å thick.

3. The method of claim 1 wherein the oxygen is implanted in step (c) to a concentration of less than about $10^{17}/cm^2$.

4. The method of claim 1 wherein the oxygen is implanted in step (c) to a concentration of between about 5E15-1E16/cm^2.

5. A method of forming a multiple-thickness oxide layer on a silicon substrate, the method comprising:

a) growing a gate oxide layer on a silicon substrate;

b) forming a polysilicon layer on the gate oxide layer;

c) patterning an implant mask layer on the polysilicon layer;

d) implanting oxygen through the polysilicon layer;

e) stripping the implant mask layer from the substrate; and

f) annealing the substrate to form a thicker gate oxide region of the gate oxide layer, the thicker gate oxide region being oxygen-implanted oxide.

6. The method of claim 5 wherein the gate oxide layer is less than about 30 Å thick immediately after step (a).

7. A method of forming a multiple-thickness oxide layer on a silicon substrate, the method comprising:

a) forming a sacrificial oxide layer on the silicon substrate;

b) patterning an implant mask layer on the silicon substrate to expose a selected first portion of the silicon substrate;

c) implanting oxygen into the selected first portion of the silicon substrate through the sacrificial oxide layer;

d) stripping the implant mask layer from the silicon substrate;

e) stripping the sacrificial oxide layer; and

f) growing an oxide layer on the silicon substrate, the oxide layer being thicker in the oxygen-implanted oxide region in the selected first portion.

8. The method of claim 7 wherein the oxide thickness varies from about 30 Å to about 50 Å.

9. The method of claim 7 wherein step c) includes implanting oxygen into a second portion of the silicon substate under the implant mask layer, the oxygen concentration in the second portion being less than the oxygen concentration in the first portion, and the oxide layer over the first portion being thicker than the oxide layer over the second portion.

10. The method of claim 9 wherein the oxide thickness varies from about 30 Å to about 50 Å.

11. The method of claim 10 wherein the oxygen is implanted in the first portion to a concentration of about 1×10^{16} atoms cm^{-2} and the oxygen is implanted in the second portion to a concentration of about 5×10^{15} atoms cm^{-2}.

12. The method of claim 11 wherein the oxide thickness is about 50 Å over the first portion, about 40 Å over the second portion, and about 30 Å where oxygen is not implanted.

13. A method of forming a multiple-thickness oxide layer on a silicon substrate, the method comprising:

a) forming a high dielectric contrast dielectric layer on a silicon substrate;

b) forming a polysilicon layer on the dielectric layer;

c) patterning an implant mask layer on the polysilicon layer;

d) implanting oxygen through the polysilicon layer;

e) stripping the implant mask layer from the substrate; and

f) annealing the substrate to form an interfacial oxide layer under the dielectric layer.

14. The method of claim 13 wherein the dielectric layer is selected from the group consisting of silicon nitride, zirconium oxide, and hafnium silicate.

15. The method of claim 13 wherein the interfacial oxide layer is less than 2 nm in thickness.

16. A semiconductor device having a gate oxide of multiple thickness, the semiconductor device comprising:

a first gate oxide region having a first thickness, and

a second gate oxide region having a second thickness, the second gate oxide region being oxygen-implanted oxide, the second thickness being greater than the first thickness.

17. The semiconductor device of claim 16 wherein the first thickness is less than about 30 Å.

18. The semiconductor device of claim 16 wherein the first thickness is less than the second thickness by less than about 20 Å.

19. The semiconductor device of claim 16 wherein the first gate oxide region is non-implanted oxide.

20. The semiconductor device of claim 16, wherein the first gate oxide is oxygen implanted oxide, the implanted oxygen concentration being less than the implanted oxygen concentration of the second gate oxide region.

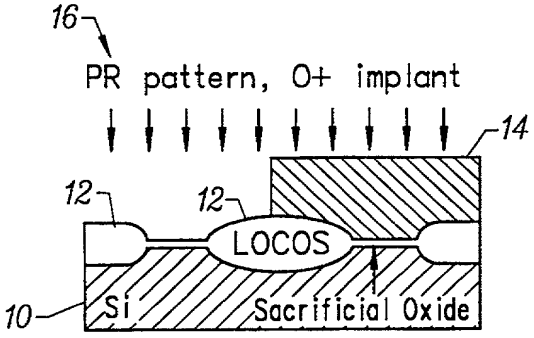

FIG. 1A

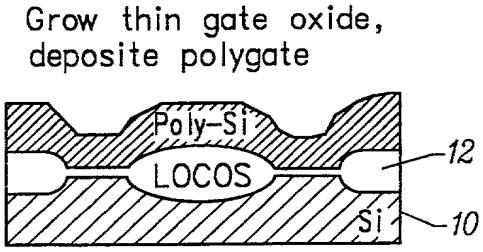

FIG. 1D

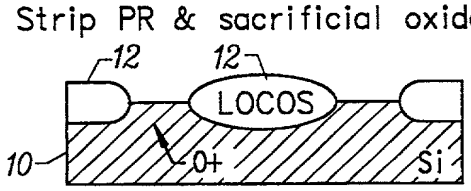

FIG. 1B

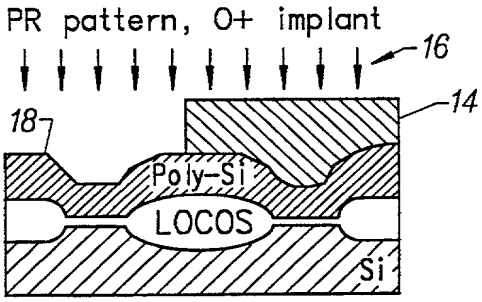

FIG. 1E

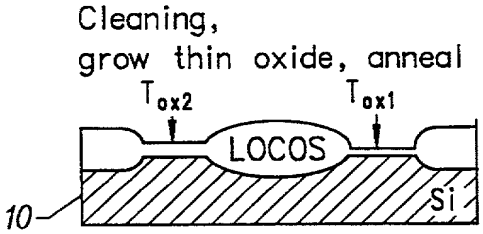

FIG. 1C

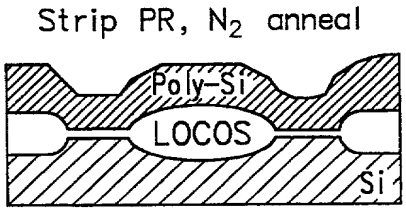

FIG. 1F

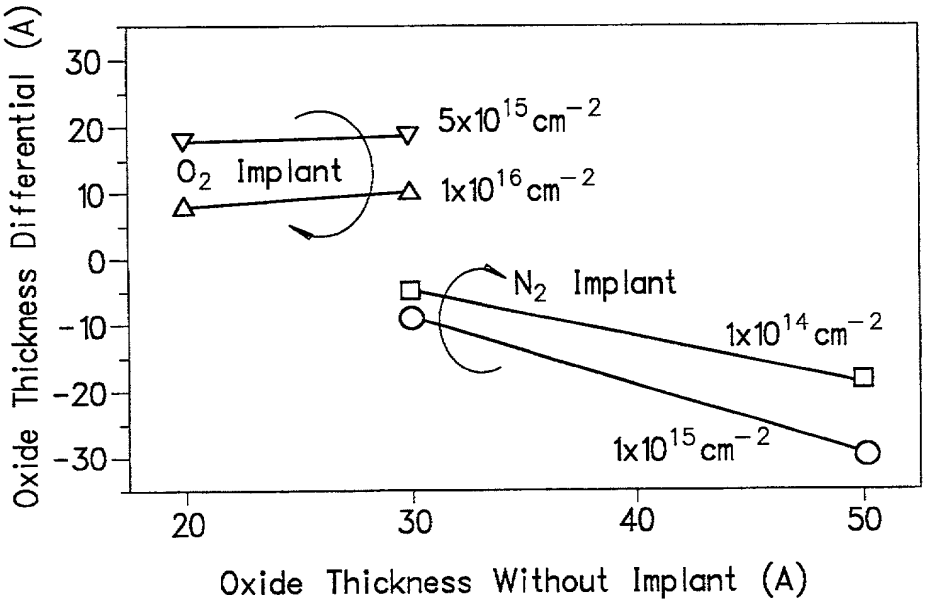
Oxide Thickness Differential (A)
30
20
10
0
-10
-20
-30
O_2 Implant
$5x10^{15}cm^{-2}$
$1x10^{16}cm^{-2}$
N_2 Implant
$1x10^{14}cm^{-2}$
$1x10^{15}cm^{-2}$
20
30
40
50
Oxide Thickness Without Implant (A)

FIG. 2

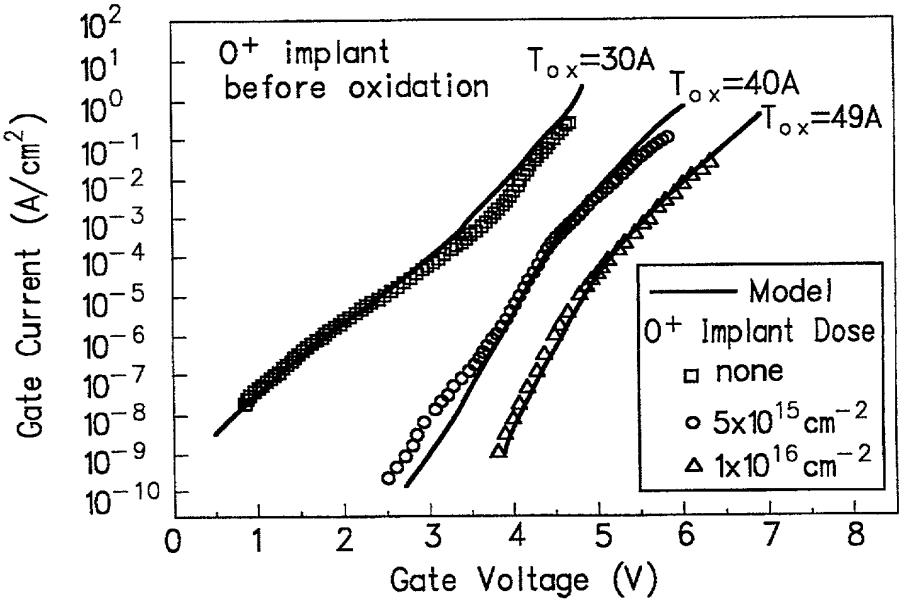
Gate Current (A/cm^2)
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
O^+ implant
before oxidation
T_{ox}=30A
T_{ox}=40A
T_{ox}=49A
Model
O^+ Implant Dose
none
$5x10^{15}cm^{-2}$
$1x10^{16}cm^{-2}$
0
1
2
3
4
5
6
7
8
Gate Voltage (V)

FIG. 3

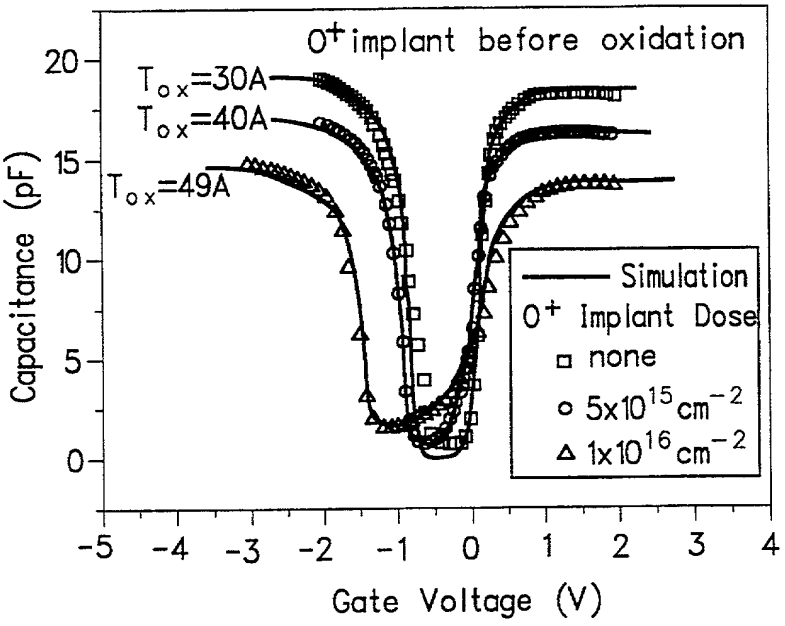
0+ implant before oxidation
Tox=30A
Tox=40A
Tox=49A
Capacitance (pF)
Gate Voltage (V)
Simulation
0+ Implant Dose
none
5x10^15 cm^-2
1x10^16 cm^-2

FIG. 4

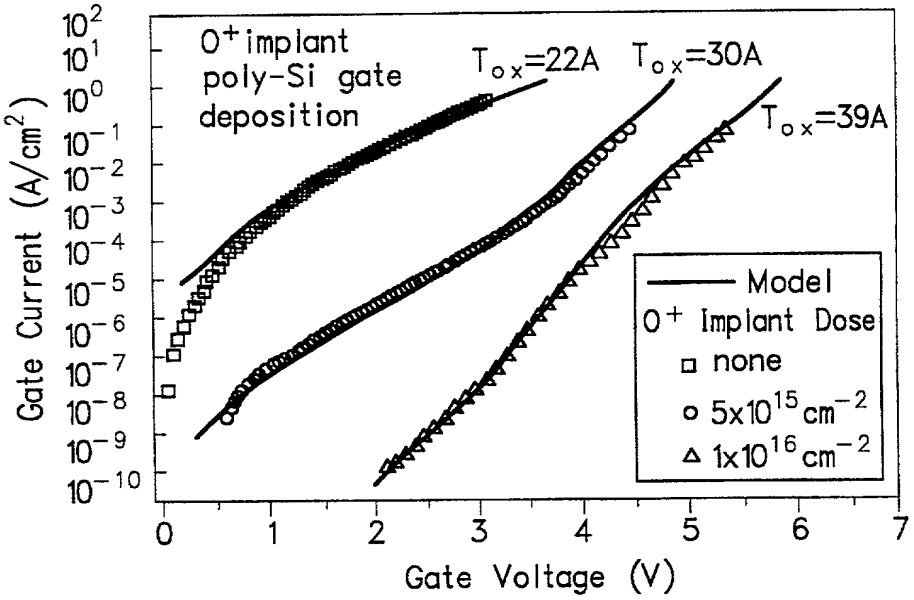
0+ implant
poly-Si gate
deposition
Tox=22A
Tox=30A
Tox=39A
Gate Current (A/cm^2)
Gate Voltage (V)
Model
0+ Implant Dose
none
5x10^15 cm^-2
1x10^16 cm^-2

FIG. 5

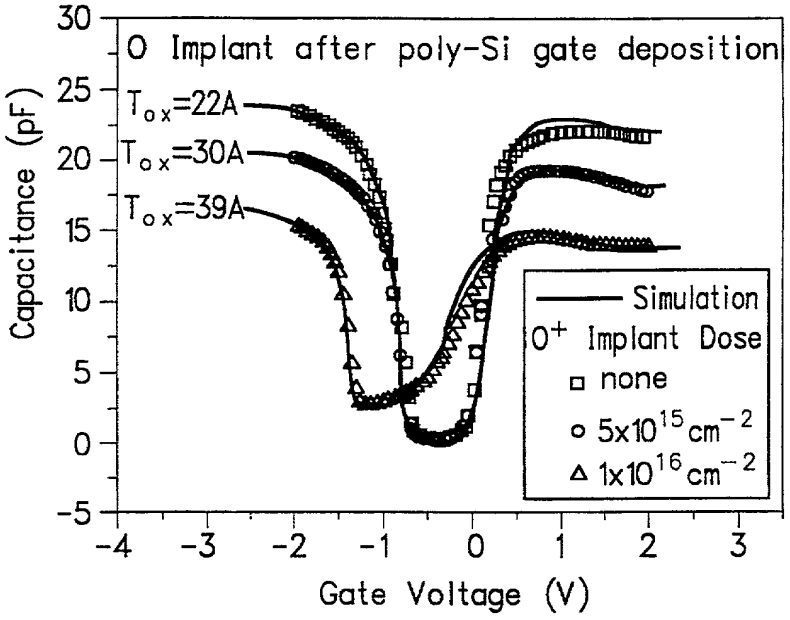
O Implant after poly-Si gate deposition
T_{ox}=22A
T_{ox}=30A
T_{ox}=39A
Capacitance (pF)
Gate Voltage (V)
Simulation
O^+ Implant Dose
none
$5x10^{15}cm^{-2}$
$1x10^{16}cm^{-2}$

FIG. 6

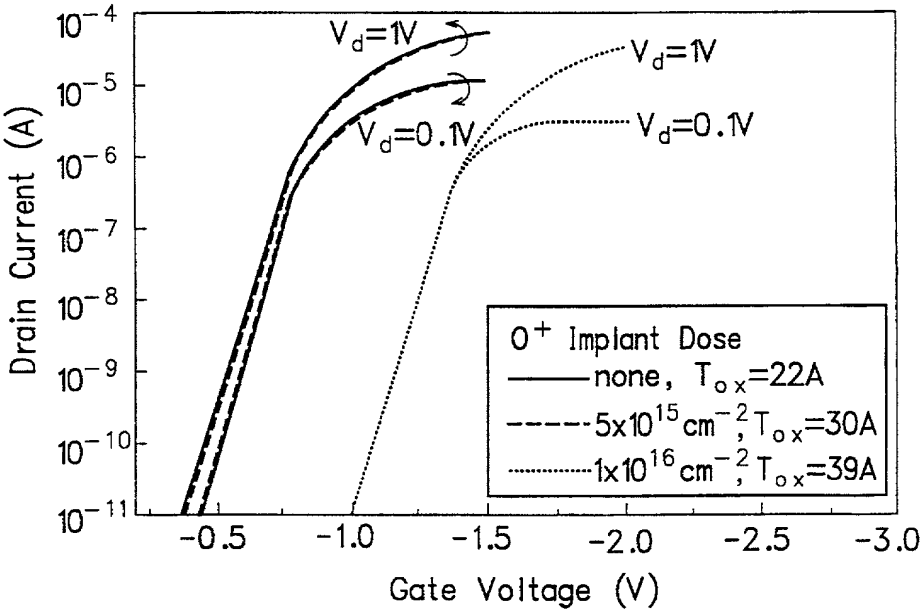
V_d=1V
V_d=0.1V
V_d=1V
V_d=0.1V
Drain Current (A)
Gate Voltage (V)
O^+ Implant Dose
none, T_{ox}=22A
$5x10^{15}cm^{-2}$, T_{ox}=30A
$1x10^{16}cm^{-2}$, T_{ox}=39A

FIG. 7

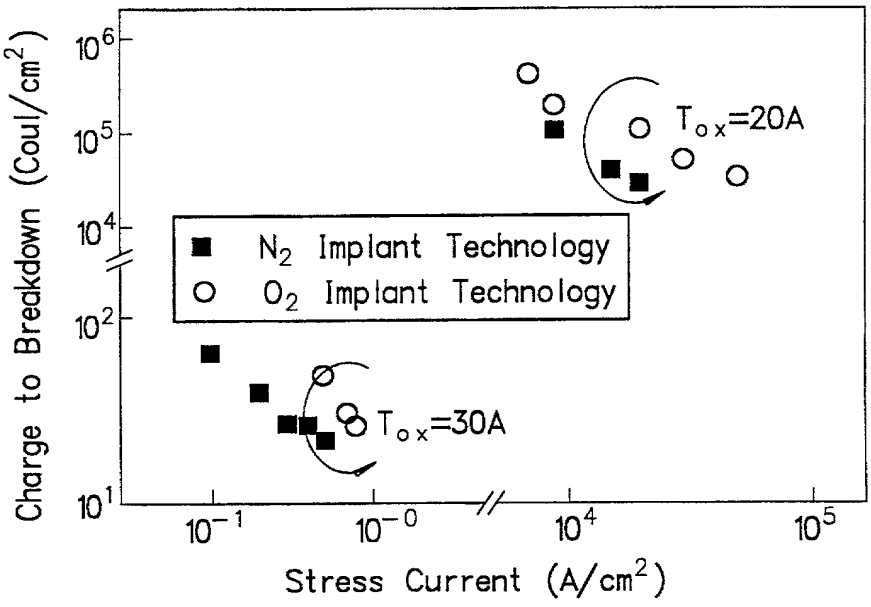
Charge to Breakdown (Coul/cm²)
Stress Current (A/cm²)
N₂ Implant Technology
O₂ Implant Technology
Tox=20A
Tox=30A

FIG. 8

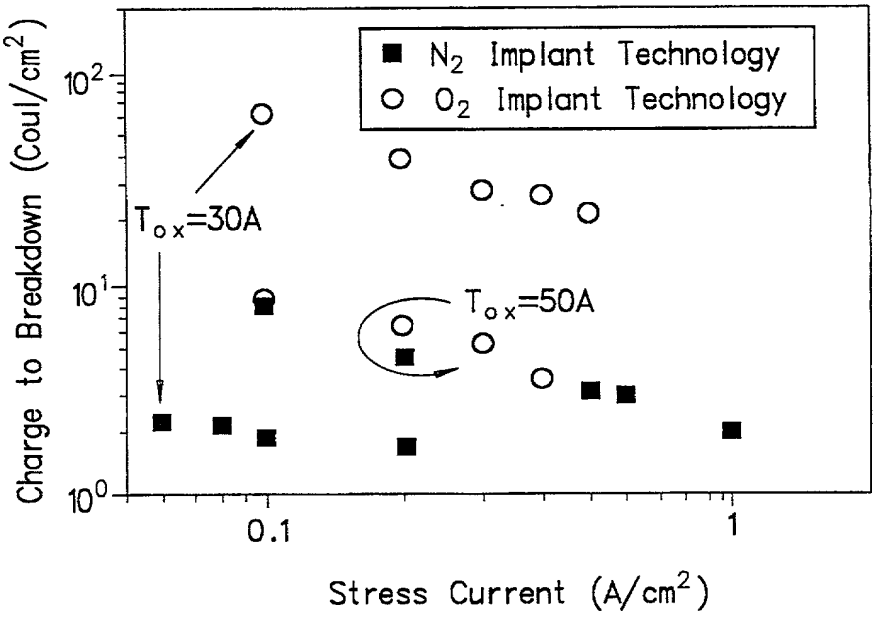
Charge to Breakdown (Coul/cm²)
Stress Current (A/cm²)
N₂ Implant Technology
O₂ Implant Technology
Tox=30A
Tox=50A

FIG. 9

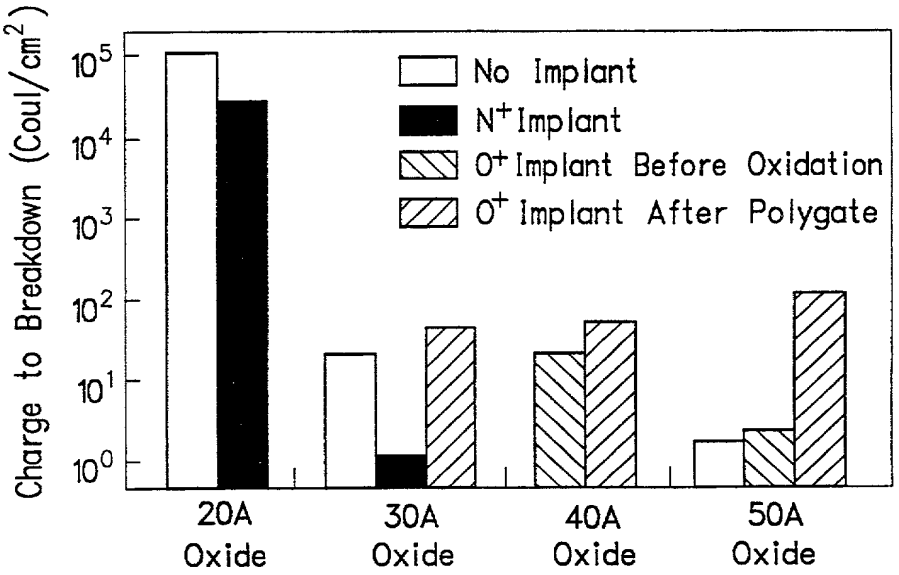
Charge to Breakdown (Coul/cm²)
10⁵
10⁴
10³
10²
10¹
10⁰
No Implant
N⁺ Implant
O⁺ Implant Before Oxidation
O⁺ Implant After Polygate
20A Oxide
30A Oxide
40A Oxide
50A Oxide

FIG. 10

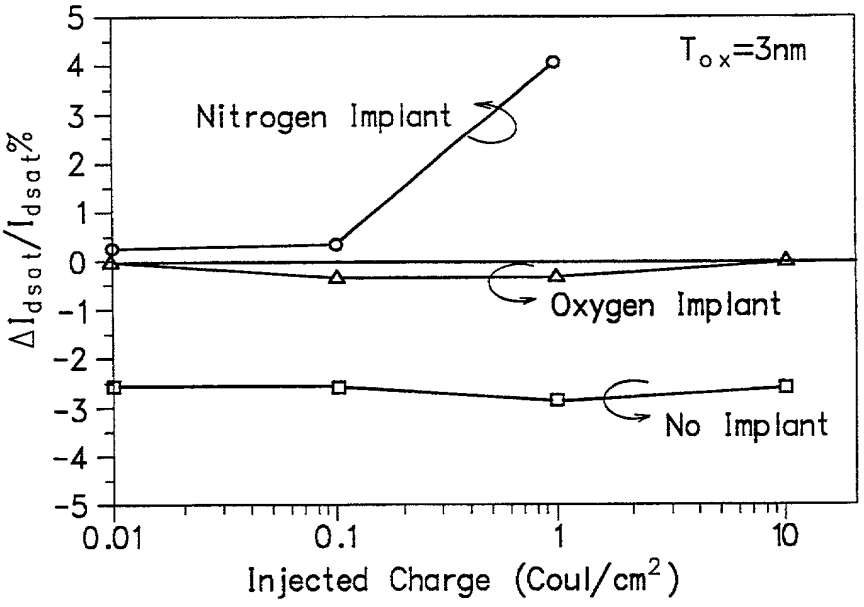
ΔIdsat/Idsat%
5
4
3
2
1
0
-1
-2
-3
-4
-5
Tox=3nm
Nitrogen Implant
Oxygen Implant
No Implant
0.01
0.1
1
10
Injected Charge (Coul/cm²)

FIG. 11

Attorney Docket No.: 015057-091620US
Client Reference No.: B99-016-2

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **MULTIPLE-THICKNESS GATE OXIDE FORMED BY OXYGEN IMPLANTATION** the specification of which ___ is attached hereto or _X_ was filed on June 4, 2001 as Application No. 09/857,453, which is the U.S. national phase of PCT/US99/28230 filed on November 29, 1999 and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119
PCT	PCT/US99/28230	November 29, 1999	Yes

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/110,885	December 4, 1998

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status
09/449,063	November 24, 1999	Pending

Full Name of Inventor 1:	Last Name: **KING**	First Name: **YA-CHIN**	Middle Name or Initial:	
Residence & Citizenship:	City: **Berkeley**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **1634 Milvia Street, Apartment 1**	City: **Berkeley**	State/Country: **California**	Postal Code: **94709**
Full Name of Inventor 2:	Last Name: **KING**	First Name: **TSU-JAE**	Middle Name or Initial:	
Residence & Citizenship:	City: **Fremont**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **470 Tumbleweed Court**	City: **Fremont**	State/Country: **California**	Postal Code: **94539**

Attorney Docket No.: 015057-091620US
Client Reference No.: B99-016-2

Full Name of Inventor 3:	Last Name: **HU**	First Name: **CHEN MING**	Middle Name or Initial:	
Residence & Citizenship:	City: **Alamo**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **2060 Pebble Drive**	City: **Alamo**	State/Country: **California**	Postal Code: **94507**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Ya-Chin King	Tsu-Jae King	Chen Ming Hu
Date	Date	Date Aug 29, 2001

PA 3163802 v1

DECLARATION

As a below named inventor, I declare that:

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Post Office Address:	Post Office Address: **1634 Milvia Street, Apartment 1**	City: **Berkeley**	State/Country: **California**	Postal Code: **94709**
Full Name of Inventor 2:	Last Name: **KING**	First Name: **TSU-JAE**	Middle Name or Initial:	
Residence & Citizenship:	City: **Fremont**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **470 Tumbleweed Court**	City: **Fremont**	State/Country: **California**	Postal Code: **94539**

Full Name of Inventor 3:	Last Name: **HU**	First Name: **CHEN MING**	Middle Name or Initial:	
Residence & Citizenship:	City: **Alamo**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **2060 Pebble Drive**	City: **Alamo**	State/Country: **California**	Postal Code: **94507**

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Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
Ya-Chin King	Tsu-Jae King	Chen Ming Hu
Date	Date August 20, 2001	Date

PA 3163802 v1

Attorney Docket No.: 015057-091620US
Client Reference No.: B99-016-2

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Application No.	Date of Filing	Status
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Residence & Citizenship:	City: **Fremont** CA	State/Foreign Country: **California**	Country of Citizenship: **United States**	
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Attorney Docket No.: 015057-091620US
Client Reference No.: B99-016-2

Full Name of Inventor 3:	Last Name: HU	First Name: CHEN MING	Middle Name or Initial:	
Residence & Citizenship:	City: Alamo CA	State/Foreign Country: California	Country of Citizenship: United States	
Post Office Address:	Post Office Address: 2060 Pebble Drive	City: Alamo	State/Country: California	Postal Code: 94507

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Signature of Inventor 1	Signature of Inventor 2	Signature of Inventor 3
X Ya-Chin King	Tsu-Jae King	Chen Ming Hu
X Date 8/15/2001	Date	Date

PA 3163802 v1